REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 1-13 and 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Cohen (U.S. Patent Publication No. 2005/0040444). Applicant respectively traverses.

Claim 1 recites that a source slot and a drain contact region are formed at opposite ends of a NAND string disposed on a substrate of the memory array using a single mask, the NAND string comprising a plurality of memory cells connected in series between a source select gate and a drain select gate, where a portion of the drain contact region is formed directly over the drain select gate and where the single mask defines areas for exposing the substrate.

Cohen shows (Figures 18-22) a plurality of field effect transistors, but does not disclose whether these field effect transistors provide any memory function. Further, it is apparent from Figure 20 that the field effect transistors are connected in parallel, and not in series, in that successive field effect transistors share source regions and drain regions. Moreover, the Examiner took an implanted source region 18A and an implanted drain region 18C (Figure 18) as respectively corresponding to the source select gate and drain select gate of claim 1. However, it is apparent from Figure 18 that source region 18A and drain region 18C function as the source and drain regions of a field effect transistor and not as source and drain select gates. Therefore, Cohen does not include each and every recitation of claim 1, so claim 1 should be allowed.

Claims 2-8 depend from claim 1 and are thus allowable for at least the same reasons as claim 1. Therefore, claims 2-8 should be allowed.

Claim 9 recites that a NAND string is disposed on the substrate, that source and drain select gates are respectively disposed on the substrate at opposite ends of the NAND string and electrically connected to the NAND string, and that the NAND string has a plurality of memory cells connected in series. As is apparent from above in conjunction with claim 1, Cohen does not include this. Therefore, Cohen does not include each and every recitation of claim 9, so claim 9 should be allowed.

Claims 10-13 and 17 depend from claim 9 and are thus allowable for at least the same reasons as claim 9. Therefore, claims 10-13 and 17 should be allowed.

Claim Rejections Under 35 U.S.C. § 103

Claims 14-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cohen (U.S. Patent Publication No. 2005/0040444). Applicant respectfully traverses.

Claim 9 is patentably distinct from Cohen. The taking of Official Notice that Cohen discloses the claimed invention except for selecting a specific material for the dielectric layer and bulk insulation layer fails to overcome the deficiencies of Cohen with respect to claim 9. Claims 14-16 depend from claim 9 and are thus allowable for at least the same reasons as claim 9. Therefore, claims 14-16 should be allowed.

Claims 18-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cohen (U.S. Patent Publication No. 2005/0040444) in view of Sakui et al. (U.S. Patent No. 6,411,548 B1). Applicant respectfully traverses.

Claims 18 and 25 each recite that a NAND string is disposed on the substrate, that source and drain select gates are respectively disposed on the substrate at opposite ends of the NAND string and electrically connected to the NAND string, and that the NAND string has a plurality of memory cells connected in series. As is apparent from above in conjunction with claim 1, Cohen does not include this. Therefore, Cohen does not include each and every recitation of claim 18 or 25, so claims 18 and 25 are patentably distinct from Cohen.

Claims 18 and 25 each further recite the following: "forming a bulk insulation layer on the dielectric layer; forming a source slot in the bulk insulation layer adjacent the source select gate and a drain contact region in the bulk insulation layer adjacent the drain select gate using a single mask disposed on the bulk insulation layer, the drain contact region formed by self aligning the drain contact region to the dielectric layer on the drain select gate, wherein a portion of the drain contact region directly overlies the drain select gate; and removing the dielectric layer from the substrate within the source slot and drain contact region to expose the substrate. Claim 18 also recites: "forming a source line in the source slot and a drain contact in the drain contact region; and forming a bit line contact in contact with the drain contact." Claim 25 further recites: "forming a polysilicon plug in the source slot in contact with the substrate and a polysilicon plug in the drain contact region in contact with the substrate; forming an electrically conducting plug on the polysilicon plug in the source slot and on the polysilicon plug in the drain contact region; and forming a bit line contact through an interlayer dielectric on the bulk insulation layer in contact with the electrically conducting plug in the drain contact region."

Sakui et al. includes a contact hole 30d (Figure 12) reaching the drain region 28d. No portion of contact hole 30d is formed directly overlying gate electrode (or select gate line) 27(SSL). In Figure 44, a contact plug 31d is formed in the contact hole 30d and is connected to an intermediate layer 33d that is connected to bit line 36(BL) through a contact plug 32d. Sakui et al. also includes a source line 33(SL) connected to a contact plug 31s formed in a contact hole 30s. However, formation of intermediate layer 33d requires a different step than the formation of contact plugs 31s and 31d. This means that Sakui et al. does not form contact holes 30s and 30d and a region directly overlying gate electrode (or select gate line) 27(SSL) using a single mask layer. Therefore, Sakui et al. does not recite or suggest each and every element of claim 18 or 25. Moreover, there is no indication Sakui et al. that there is anything wrong the method of Sakui et al., so there is no motivation for changing the of Sakui et al. This means that Cohen in combination with Sakui et al. fails to overcome the deficiencies of Cohen with respect to claims 18 and 25, so claims 18 and 25 should be allowed.

Claims 19-24 depend from claim 18 and are thus allowable for at least the same reasons as claim 18. Claims 26-28 depend from claim 25 and are thus allowable for at least the same reasons as claim 25. Therefore, claims 19-24 and 26-28 should be allowed.

Allowable Subject Matter

Applicant acknowledges that claims 42-62 were allowed.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2208.

Respectfully submitted,

Date: 10-26-06

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